Abstract

A structure and method for fabricating integrated circuits with improved electrical performance.

The structure comprises electronic devices formed along a semiconductor surface, a first upper level of interconnect members over the semiconductor surface, a lower level of interconnect members formed between the semiconductor surface and the first upper level, and insulative material positioned to electrically isolate portions of the upper level of interconnect members from one another. The insulative material comprises a continuous layer extending from within regions between members of the upper interconnect level to within regions between members of the lower interconnect level and is characterized by a dielectric constant less than 3.9.

The method begins with a semiconductor layer having electronic device regions thereon. A first insulative layer is deposited over the electronic device regions and a lower level of interconnect members is formed over the first insulative layer. A second insulative layer is formed between and over lower level interconnect members and an upper level of interconnect members is formed over the second insulative layer. Portions of the second insulative layer positioned between interconnect members of the lower and upper levels are removed and a third insulative layer is formed in regions from which the second insulative layer is removed.